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Remarks

Claims 2, 6-8, 25-36, 47, 49-51, 53-57, and 63 are pending in the present application. Withdrawn claims 50, and 60-62 are now canceled. New claim 63 has been added. No new matter has been entered.

Double Patenting Rejection

Claims 2, 6, 8, and 57 were rejected under the judicially created doctrine of obviousness-type double patenting based on claims 1-16 of Vaiyapura (U.S. 6,507,107) further in view of Suzuki (U.S. 5,532,910). However, Vaiyapura cannot be asserted against the claimed invention, because Vaiyapura does not constitute prior art. The present application has a filing date of March 12, 2001, wherein the Vaiyapura reference has a U.S. filing date of May 15, 2001, and foreign priority date of March 15, 2001. Consequently, the present application has a filing date of March 12, 2001 that predates the Vaiyapura priority date of March 15, 2001; therefore, the Vaiyapura reference does not constitute prior art under § 102. Accordingly, the rejection for double patenting should be removed.

Rejection under § 103

Claims 2, 6, 8, 25-36, 47, 49-51, 53-57 were rejected under § 103(a) based on the combination of Lo (U.S. 6,507,098) and Suzuki. To establish a prima facie case of obviousness, three basic criteria must be met. See MPEP 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make

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the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Independent claims 2, 6-8, 49, and 50 recite a multiple die semiconductor assembly comprising, *inter alia*, a first semiconductor die, a second semiconductor die and an intermediate substrate positioned between the first semiconductor die and the second semiconductor die. The multiple die semiconductor assembly further comprises at least one decoupling capacitor conductively coupled to at least one of the first and/or second semiconductor dies.

Lo is cited for teaching a multi-chip packaging structure having a first chip 26, second chips 40 and 42, and a substrate 10. The examiner concedes that Lo's structure fails to include decoupling capacitors. To cure this noted deficiency, the examiner modifies the teachings of Lo by incorporating the decoupling capacitor of Suzuki into Lo's multichip packaging structure. The examiner asserted it would be obvious to incorporate the decoupling capacitor into the Lo structure to remove electric noise.

None of the cited references, singularly or in combination, teach all elements of the claims. Specifically, Suzuki teaches decoupling capacitors; however, Suzuki does not teach decoupling capacitors coupled to a first or second semiconductor die. The Suzuki decoupling capacitor is bonded to a conductive copper lead frame, not a semiconductor die. The placement of decoupling capacitors is essential for the functionality for the present invention. For example, each decoupling capacitor 60 may be placed in an electrical circuit between the high and low voltage inputs of one of the dies 20, 30. *See generally* [0028]. In this manner, the decoupling capacitors 60 decouple the low voltage input from the high voltage input on one of the dies, thereby serving as a power source filter or surge/spike suppressor. *Id.* Accordingly, the cited

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references, alone or in combination, fail to teach a decoupling capacitor coupled to a semiconductor die.

Furthermore, there is no reasonable expectation of success or motivation to combine the teachings of Lo and Suzuki in order to teach the claimed invention. As stated above, Suzuki teaches a decoupling capacitor bonded to a *conductive* copper lead frame. The prior art does not teach that incorporating the decoupling capacitor into a *semiconductor* die will have a reasonable expectation of success. Suzuki does not disclose that decoupling capacitors are effective at various voltages and currents. Moreover, the examiner asserts that Suzuki suggests the combination of Lo and Suzuki by stating that decoupling capacitors may remove electric noise. The Suzuki conductive lead frame may encounter electric noise, because it is an electrically conductive material. However, our invention does not disclose that electric noise is a problem to be resolved. If electric noise was a problem in our invention to be solved, one skilled in the art would resolve the electric noise problem at the source i.e. by coupling the decoupling capacitor to the conductive lines or frames. In contrast, semiconductor dies are less conductive than copper lead frames and will encounter less electric noise; therefore, one skilled in the art would not be led to couple the capacitors to semiconductor dies, as recited in the claimed invention. Thus, there is no motive to combine Lo and Suzuki, and there is no reasonable expectation of success in modifying the Lo and Suzuki references to teach the claimed invention. Accordingly, the combination of Lo and Suzuki fails to establish a prima facie case of obviousness.

The Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application

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or of this response. Otherwise, early notification of allowable subject matter is respectfully requested.

Respectfully submitted,

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